PS/2 Keyboard Interface for the XSA Boards

October 21, 2004 (Version 1.0) Application Note by D. Vanden Bout

Summary

This application note discusses the serial data stream that arrives from a PS/2 keyboard and describes a simple circuit that lets the XSA Board capture keystrokes.

PS/2 Keyboard Interface Features

- Captures serial transmissions of scancodes from a PS/2 keyboard and presents them as parallel bytes.
- Provides status information that indicates when the interface is busy receiving a scancode and when the scancode reception is complete.
- Indicates if errors occur during reception.

Principles of the PS/2 Keyboard

A PS/2 keyboard connects to the XSA Board through two signals:

1. A data signal carries a serial stream of bits from the keyboard as each key is pressed and released. Each key is assigned an eight-bit scancode that is transmitted least-significant bit to most-significant bit with a preceding start bit and a terminating parity bit and stop bit.
2. A clock signal is output by the keyboard and the falling edge of this signal indicates when to sample the logic level on the data signal.

The keyboard interface accepts the serial data stream and outputs the eight-bit scancode in parallel along with a ready pulse that indicates a valid scancode is available. An additional busy signal goes high as the bits are received. The ready pulse is generated after 11 bits have been received (start bit + 8 data bits + parity bit + stop bit) and the clock signal goes high and stays there. The sequencing of these signals is shown in Figure 1.

A single scancode is transmitted when a key is pressed. But two scancodes are transmitted when the key is released: an initial scancode of 11110000 to indicate the key release, and then the scancode for the key is sent again. The keyboard interface generates the ready pulse only after the key has been released.

PS/2 Keyboard Interface Parameters and I/O

Generic Parameters

The following generic parameter affects the operation of the PS/2 keyboard interface:

FREQ: This parameter sets the main operating frequency of the interface. This frequency is used to calculate the timeout value that determines when ps2_clk has stopped pulsing. The timeout value is determined by dividing the main clock frequency by the frequency of ps2_clk. If the main clock is 50 MHz and the keyboard clock is 10 KHz, then the timeout value is 5000 which means ps2_clk is seen as static if it remains high for 5000 pulses of the main clock.

I/O Ports

The I/O ports for the PS/2 keyboard interface are shown in Figure 2. The functions of the ports are as follows:

rst: This active-high, asynchronous input resets the internal circuitry of the sync generators.

clk: This is the main clock input. The clock from the external oscillator enters the FPGA through a global clock input pin and drives this input.

ps2_clk: The clock signal from the PS/2 keyboard enters through this port.

ps2_data: This input accepts the serial data from the PS/2 keyboard.

scancode: The received scancode is output through this eight-bit parallel output.

parity: The parity bit received at the end of the scancode is output on this port.

busy: This status output goes high as bits are received through the scancode port.

rdy: This status output pulses high for a single clock cycle when a complete scancode has been received.

error: This status output is driven high if the PS/2 clock signal stays low for too long or if it stops pulsing before an entire scancode is received.

PS/2 Keyboard Test Application

A simple application of the PS/2 keyboard interface uses it to display any of the 0-9 digits that are pressed.

Figure 2 shows the connections between a PS/2 keyboard, the interface and a seven-segment LED. When a key is pressed and released, the serially transmitted scancode is presented in parallel on the scancode output bus. The scancode is passed through a combinatorial mapping circuit that translates scancodes for the digit keys into an activation pattern for the seven-segment LED. This pattern is loaded into a register when the rdy output from the keyboard interface is high. Also, the connection from the error output to the reset input will reset the keyboard interface to its initial state if it detects any errors while receiving scancodes.

The source files for this application can be found at http://www.xess.com/projects/an-102104-keybrd.zip.

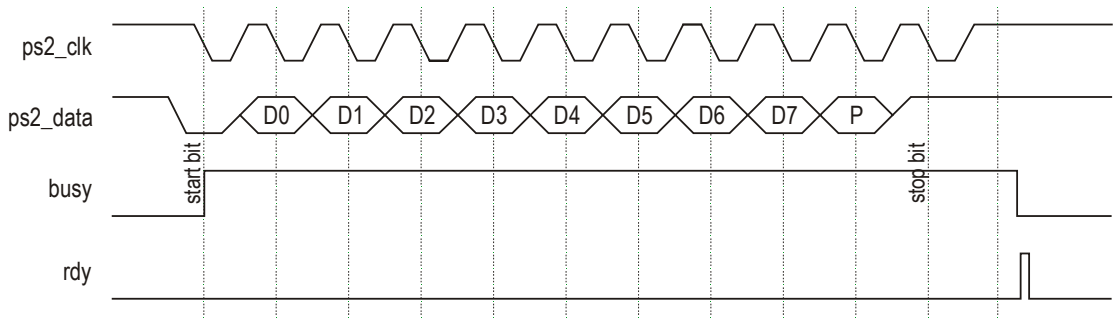

Figure 1: PS/2 keyboard waveforms.

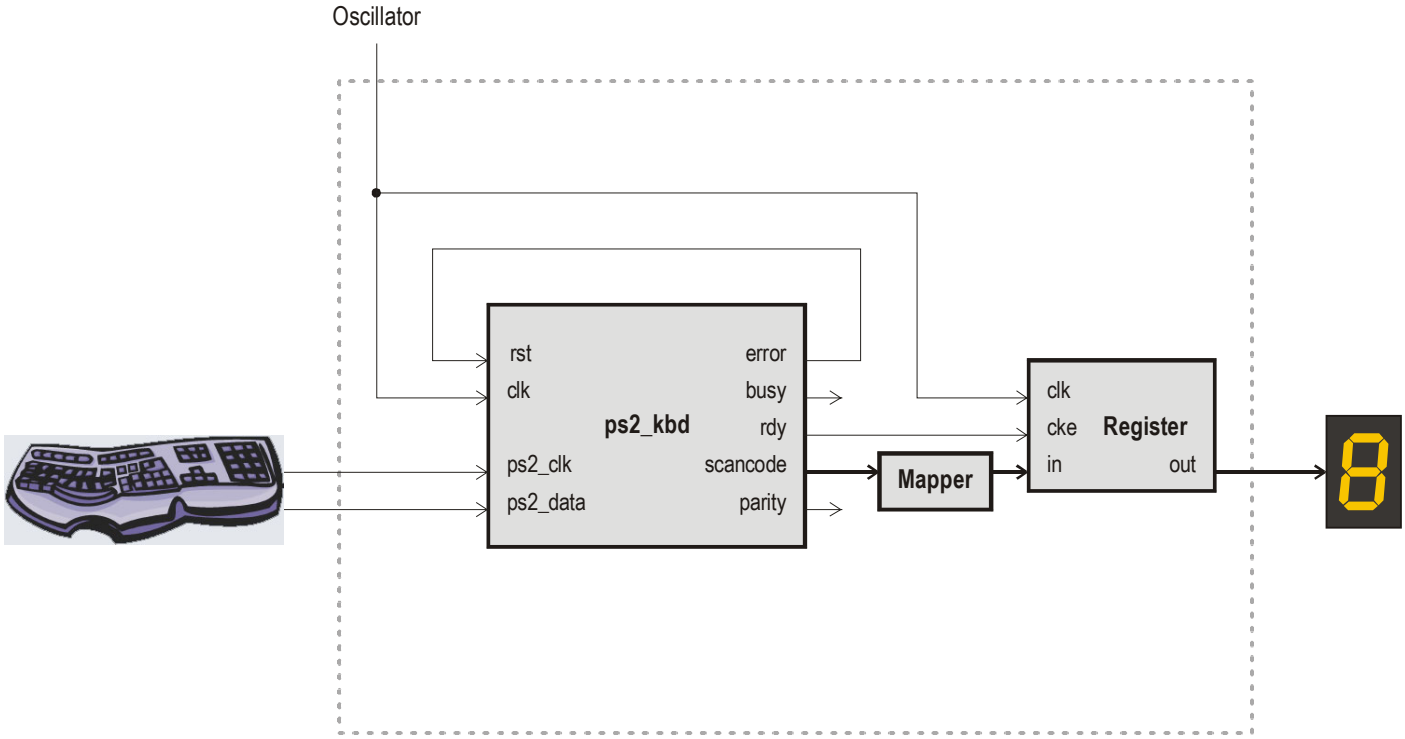

Figure 2: Using the PS/2 keyboard interface to display typed digits.

Revision	Date	Comments
1.0	10/21/04	Initial version.