Using the XSV Board Xchecker Interface

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Summary

This application note shows how to configure the XC95108 CPLD on the XSV Board to enable the programming and JTAG functions of the Xchecker interface.

Introduction

The Virtex FPGA on the XSV Board is accessed from the PC parallel port through a simple 25-wire cable that connects to an XC95108 CPLD on the XSV Board. The connections of the CPLD to the configuration and JTAG pins of the Virtex device are shown in Figure 1. The XSV Board is supplied with a default CPLD configuration that lets you download bitstreams to the Virtex using the GXSLOAD utility provided by XESS.

This application note describes an alternate circuit for the CPLD that allows you to use all the Xilinx Foundation downloading and testing tools with the XSV Board by attaching an Xchecker cable to the Xchecker interface on the XSV Board.

VHDL for the Xchecker Interface

Listing 1 shows the VHDL code for the XC95108 CPLD that enables the Xchecker interface on the XSV Board. This interface provides two functions:

- It transfers configuration bitstreams from the PC to the Virtex FPGA using the slave-serial mode.
- The JTAG signals can be used to readback and/or test the FPGA.

How the VHDL implements these functions is described below.

Line 27 drives the mode pins of the Virtex FPGA to set it in the slave-serial configuration mode. This is appropriate if you want to download bitstreams to the Virtex device through its dedicated programming pins (CCLK, DONE, DIN, /PROG, and /INIT). The levels on the mode pins can be changed to enable configuration of the FPGA through the JTAG pins (TCK, TMS. TDO, and TDI).

Line 30 disables the Flash RAM because the data outputs of the Flash (D0–D3) can interfere with Virtex DIN signal and the TMS, TDO, and TDI JTAG signals. Note that pin 170 of the Virtex also connects to the Flash chip-enable input, so this FPGA pin cannot be used as an output due to contention. In addition, pins 156, 163, and 167 of the FPGA also connect to the TMS, TDO, and TDI signals so they must remain tristated if the JTAG features of the Xchecker interface are used.

Line 36 makes the CPLD pass the value from the TDO pin of the Virtex FPGA over to the RD pin of the Xchecker interface. Note that pin 163 of the FPGA is also connected to TDO and pin 133 is connected to the RD pin of the Xchecker interface, so these pins on the FPGA must be tristated to prevent contention with the TDO output to the Xchecker interface.

Line 39 causes the FPGA DONE signal to be displayed on the uppermost segment of the bargraph LED. The bar segment is illuminated after the Virtex FPGA is configured and its DONE signal is high. Pin 152 of the FPGA must be tristated to prevent contention with the CPLD when it is driving this LED.

The remaining pins of the CPLD are unused so they are tristated and will not interfere with the remaining signals of the Xchecker interface or the FPGA.

The I/O pin assignments for the CPLD on the XSV Board are shown in Listing 2.

Using the Xchecker Cable with the XSV

First, attach the XSV Board to the parallel port of a PC through the 25-wire downloading cable. Then download the xchk.svf file into the XC95108 CPLD

using the GXSLOAD tool from XESS. At this point, the parallel port interface of the XSV Board is no longer functioning (unless you reprogram the CPLD) and the Xchecker interface is active.

Next, connect the Xchecker cable to a serial port of the PC. Then connect the other end of the Xchecker to the XSV Board (the Xchecker connections are keyed so they cannot be attached incorrectly).

Next, click-on the Programming tools icon in Foundation and select the Hardware Debugger tool. Select the Cable➔Communications... menu item in the Hardware Debugger window and set the Cable Type to Xchecker. Then set the Port Name to com1 (or whatever COM port the Xchecker cable connects to) and the Baud Rate to 38400.

Once the cable is set up, select a .BIT file in the Hardware Debugger window and download it to the XSV Board. After the download is complete, the status information at the bottom of the window should show the FPGA is configured. BAR0 on the XSV Board should also be illuminated.

Now click-on the Programming tools icon but this time select the JTAG Programmer tool. Select the Output➔Cable Setup... menu item in the JTAG Programmer window and set the Communication Mode to Xchecker, the Port to com1, and the Baud Rate to 38400. Then select the Output➔Cable Reset command to initialize the JTAG state machine in the Virtex FPGA. Now you can execute JTAG operations on the Virtex FPGA.

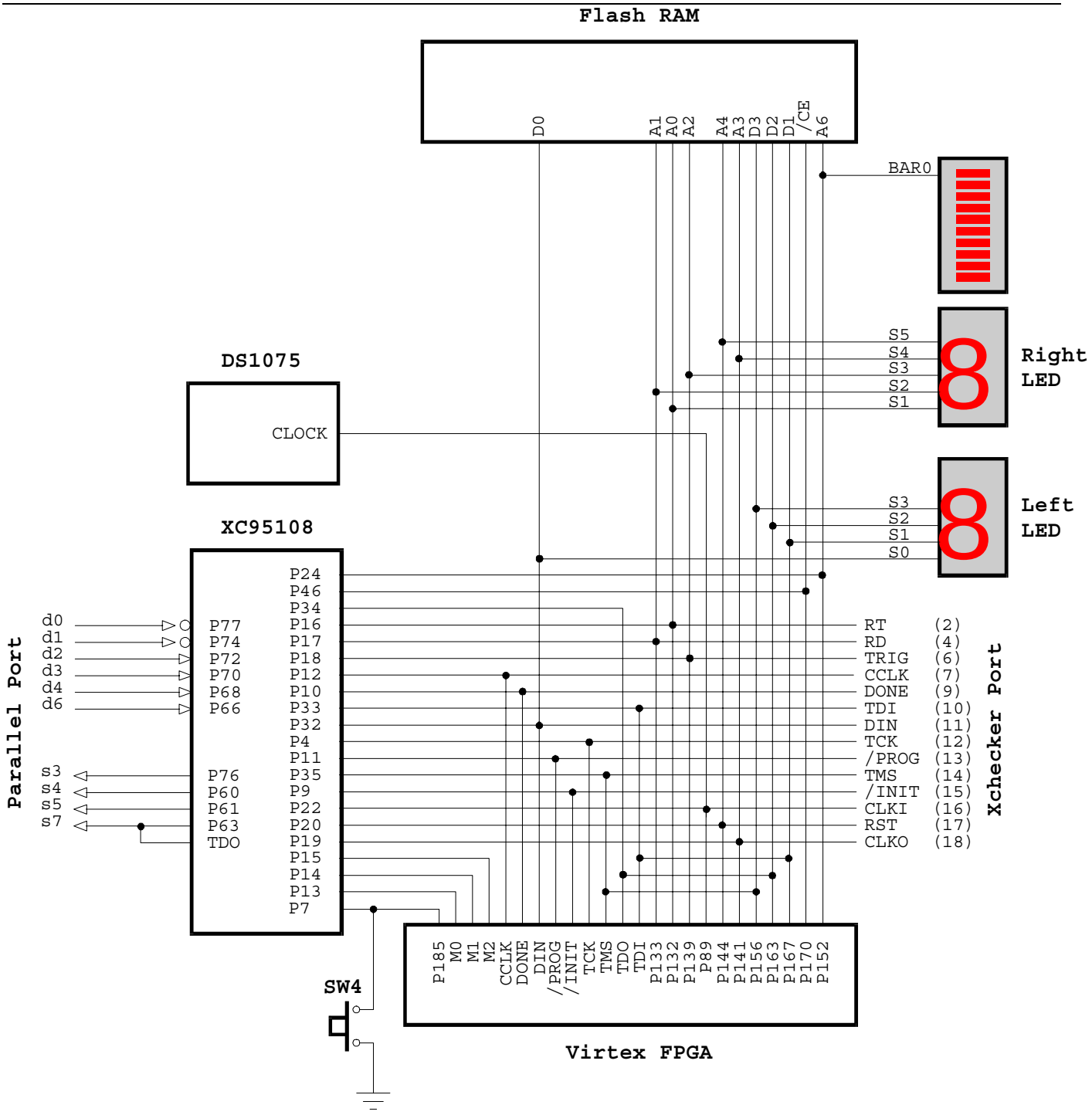

Figure 1: XSV Board CPLD connections.

Listing 1: VHDL code for the CPLD that enables the XSV Xchecker interface.

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity xchk is
5     port(
6        ce_n:   out   std_logic; -- Flash RAM chip-enable
7
8        V_tdo:  in    std_logic; -- TDO from Virtex FPGA
9        V_rd:   out   std_logic; -- RD pin of xchecker port used for TDO
10
11       -- Virtex programming pins
12       V_done: in    std_logic; -- input from Virtex done pin
13       V_m:    out   std_logic_vector(2 downto 0);-- Virtex config mode pins
14
15       bar:    out   std_logic_vector(1 downto 0)  -- LED bargraph
16    );
17 end xchk;
18
19
20 architecture arch of xchk is
21    constant LO: std_logic := '0';
22    constant HI: std_logic := '1';
23    constant SLAVE_SERIAL_MODE: std_logic_vector(2 downto 0) := "111";
24 begin
25
26    -- connect Virtex configuration pins
27    V_m <= SLAVE_SERIAL_MODE;  -- set Virtex config mode pins into JTAG mode
28
29    -- disable the Flash RAM so its outputs cannot interfere with the JTAG pins
30    ce_n <= HI;
31
32    -- loop Virtex TDO output pin over to RD pin on the Xchecker interface
33    -- Note: V_tdo is also connected to Virtex pin 163 and V_rd is
34    -- connected to Virtex pin 133, so keep these two Virtex pins
35    -- tristated if you are using the XChecker JTAG interface to the Virtex.
36    V_rd <= V_tdo;
37
38    -- display status of Virtex done pin on the bargraph LED
39    bar(0) <= V_done;
40
41 end arch;
```

Listing 2: User-constraint file for CPLD pin assignments.

```
1  #
2  # pin assignments for the XC95108 CPLD chip on the XSV Board
3  #
4
5  net V_done    loc=p10;
6  net V_m<0>    loc=p13;
7  net V_m<1>    loc=p14;
8  net V_m<2>    loc=p15;
9  net V_tdo     loc=p34;
10 net V_rd      loc=p17;
11 net ce_n      loc=P46;
12 net bar<0>    loc=p24;
```